WHAT IS CLAIMED IS:

1. A lateral metal-oxide semiconductor field effect transistor (MOSFET), comprising:

a silicon carbide layer located over or within a substrate of a semiconductor wafer, a gate formed on the silicon carbide layer; and

source and drain regions located in the silicon carbide layer and laterally offset from the gate.

2. The MOSFET as recited in Claim 1 wherein the silicon carbide layer has a breakdown voltage greater than a breakdown voltage of silicon.

3. The MOSFET as recited in Claim 2 wherein the silicon carbide layer has a breakdown voltage of at least about 10 volts.

4. The MOSFET as recited in Claim 1 wherein the source and drain regions are doped with an N-type dopant.

5. The MOSFET as recited in Claim 1 wherein the source and drain regions are formed in a tub doped with a P-type dopant.

6. The MOSFET as recited in Claim 1 further comprising a buried oxide layer formed in the substrate.

7. The MOSFET as recited in Claim 1 wherein the silicon carbide layer is formed on the substrate.

8. The MOSFET as recited in Claim 7 wherein the substrate comprises silicon and the silicon carbide is a 3C silicon carbide.

9. The MOSFET as recited in Claim 1 wherein the MOSFET is located on a semiconductor wafer that includes a CMOS device.

10. The MOSFET as recited in Claim 1 wherein the MOSFET is a power switch employed in a power train of a power converter.

11. A method of forming a lateral metal-oxide semiconductor field effect transistor (MOSFET) over or within a substrate of a semiconductor wafer, comprising:

forming a silicon carbide layer over the substrate;

forming a gate on the silicon carbide layer; and

forming source and drain regions in the silicon carbide layer laterally offset from the gate.

12. The method as recited in Claim 11 further comprising annealing the source and drain regions at about 1200° C.

13. The method as recited in Claim 11 further comprising forming a buried oxide layer.

14. The method as recited in Claim 13 wherein forming a buried oxide layer includes forming a buried oxide layer in the substrate.

15. The method as recited in Claim 11 wherein forming source and drain regions comprises implanting an N-type dopant into the silicon carbide layer.

16. The method as recited in Claim 11 wherein forming source and drain regions comprises forming the source and drain regions in a tub doped with a P-type dopant.

17. The method as recited in Claim 11 wherein forming a silicon carbide layer includes forming the silicon carbide layer on the substrate.

18. The method as recited in Claim 17 wherein forming a silicon carbide layer on the substrate includes forming a 3C silicon carbide layer on a silicon substrate.

19. The method as recited in Claim 11 further comprising configuring the MOSFET as a power switch and integrating the MOSFET into a power converter.

20. The method as recited in Claim 11 wherein forming a MOSFET includes forming the MOSFET on a semiconductor wafer that includes a CMOS device.

21. A power converter, comprising:

an isolation transformer;

a primary side power switch coupled to a primary winding of the isolation transformer, and a secondary side power switch coupled to a secondary winding of the isolation transformer, wherein at least one of the primary side power switch or the secondary side power switch is a lateral metal-oxide semiconductor field effect transistor (MOSFET) formed over or within a substrate of a silicon wafer;

a drive circuit coupled to the secondary side power switch and including a complementary metal oxide semiconductor (CMOS) device formed on a silicon substrate and having an operating voltage, the MOSFET having a breakdown voltage higher than the operating voltage of the CMOS device;

an output inductor coupled to the secondary side power switch; and

an output capacitor coupled to the output inductor.

22. The power converter as recited in Claim 21 wherein the MOSFET includes:

a silicon carbide layer located over or within the substrate, a gate formed on the silicon carbide layer, and

source and drain regions located in the silicon carbide layer and laterally offset from the gate.

23. The power converter as recited in Claim 21 wherein the operating voltage ranges from about 3 volts to 5 volts and the breakdown voltage ranges from about 10 volts to 30 volts.

24. The power converter as recited in Claim 21 further comprising a buried oxide layer.

25. The power converter as recited in Claim 24 wherein the buried oxide layer is located in the substrate.

26. The power converter as recited in Claim 21 wherein the source and drain regions are doped with an N-type dopant.

27. The power converter as recited in Claim 21 wherein the silicon carbide is 3C silicon carbide.

28. The power converter as recited in Claim 21 wherein the source and drain regions are formed in a tub doped with a P-type dopant.

29. The power converter as recited in Claim 21 wherein the silicon carbide layer is formed on the silicon substrate.

30. The power converter as recited in Claim 21 wherein the gate comprises polysilicon and the substrate comprises silicon doped with a P-type dopant.

31. A method of forming a power converter, comprising:

forming an isolation transformer;

forming a primary side power switch coupled to a primary winding of the isolation transformer;

forming a secondary side power switch coupled to a secondary winding of the isolation transformer, at least one of the primary side power switch and the secondary side power switch being a lateral metal-oxide semiconductor field effect transistor (MOSFET) formed over or within a substrate of a silicon wafer;

forming a drive circuit coupled to the secondary side power switch and including a complementary metal oxide semiconductor (CMOS) device formed on a silicon substrate and having an operating voltage, the MOSFET having a breakdown voltage higher than the operating voltage of the CMOS device;

forming an output inductor coupled to the secondary side power switch; and

forming an output capacitor coupled to the output inductor, the secondary side power switch.

32. The method as recited in Claim 31 wherein forming a MOSFET includes:

forming a silicon carbide layer over or within the substrate;

forming a gate on the silicon carbide layer; and

forming source and drain regions in the silicon carbide layer and in contact with the gate.

33. The method as recited in Claim 31 further comprising annealing the source and drain regions at about 1200° C.

34. The method as recited in Claim 31 further comprising forming a buried oxide layer.

35. The method as recited in Claim 34 wherein forming a buried oxide layer includes forming a buried oxide layer in the substrate.

36. The method as recited in Claim 31 wherein forming the source and drain regions comprises implanting an N-type dopant into the silicon carbide layer.

37. The method as recited in Claim 31 wherein forming the source and drain regions comprises forming the source and drain regions in a tub doped with a P-type dopant.

38. The method as recited in Claim 31 wherein forming a silicon carbide layer includes forming the silicon carbide layer on the substrate.

39. The method as recited in Claim 31 wherein forming the silicon carbide layer on the substrate includes forming the silicon carbide layer on a silicon substrate.

40. The method as recited in Claim 31 further comprising forming an oxide layer over the silicon carbide layer employing chemical vapor deposition.

41. The method as recited in Claim 40 further comprising annealing the oxide layer at about 950° C.

42. The method as recited in Claim 31 wherein forming a silicon carbide layer includes forming a 3C silicon carbide layer.

43. The method as recited in Claim 31 wherein forming a CMOS device includes forming the CMOS device to have an operating voltage ranging from about 3 volts to about 5 volts and forming a MOSFET includes forming a MOSFET having a breakdown voltage ranging from about 10 volts to about 30 volts.

add C'

add D'